LM1290

Autosync Horizontal Deflection Processor

General Description

The LM1290 is a high performance, low cost deflection circuit solution for autosync monitors.

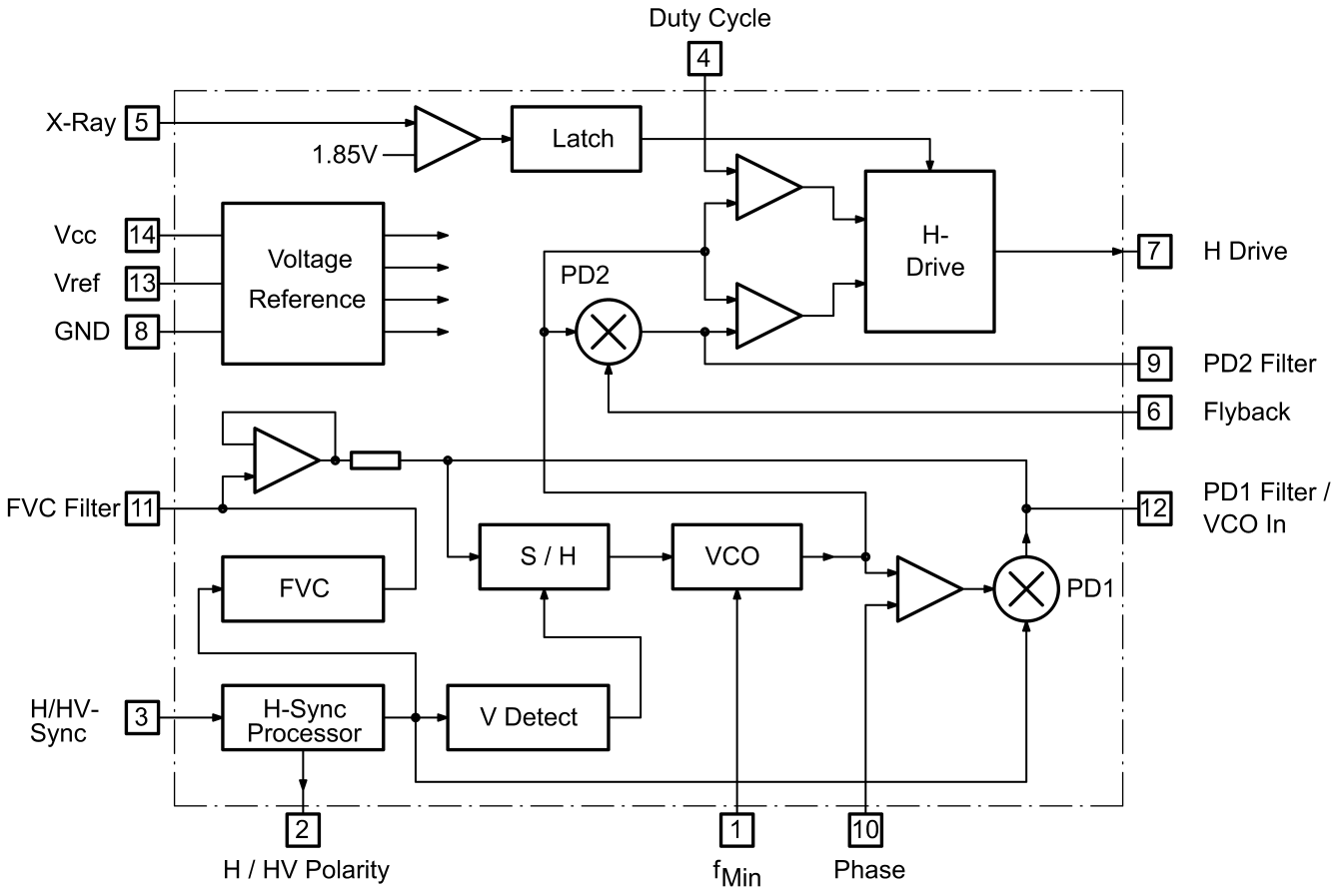
The LM1290 provides full autosync capability, DC controls and complete freedom from manufacturing trims. Its continous capture range is from 22kHz to 110kHz (1:5). Mode change frequency ramping, for protection of the horizontal deflection output transistor, is programmable by using an external capacitor.

Together with the National Semiconductor LM1296 Raster Geometry Correction System for Multisync-Frequency Displays, excellent performance is offered. The two-chip solution provides the advantage of good jitter performance, simplified board layout and lower system costs.
The LM1290 is packaged is a 14-pin plastic DIP package.

Plastic DIP-14 (LM1290N)

Features

- Full autosync - 22kHz to 110kHz with no component switching or external adjustements
- No manufacturing trims needed - internal VCO capacitor trimmed on chip
- Sample-and-Hold circuit for fast top-of-screen phase recovery, even when using composite sync.
- DC-controlled H phase and duty cycle
- Resistor-programmable minimum VCO frequency
- Excellent jitter performance
- X-ray input disables H drive until V_{CC} powered down
- Low V_{CC} disables H drive (VCC < 8.5V)
- H output transistor protected against accidental return on during fly back
- Capacitor-programmable frequency ramping, df_{VCO} / dt, protects H output transistor during scanning mode changes



Electrical Characteristics

T_A = 25°C, V_{CC} = 12V, V_5 = 0V unless otherwise stated.

Parameter	Condition	Typical (Note 6)	Limit (Note 7)	Units
Supply Current (Pin14)	PIN 3 and PIN 7 Open Circuit, Pin 1 = -100µA	30	40	mA (max)
Minimum Capture Frequency	H Sync Duty Cycle = 10%; Pin 1 (f_{MIN}) Open	10	22	kHz (max)
Maximum Capture Frequency		115	110	kHz (max)
H / HV Sync Input (Pin3) Threshold Voltage	High Level		2.2	V (min)
	Low Level		0.8	V (max)
H / HC Sync Input (Pin3) Maximum Sync Tip Duty Cycle		26	24	%
H / HC Sync Input (Pin3) Minimum Sync Tip Duty Cycle	f_H = 22kHz	5		%
H / HV Polarity (Pin2) Low Level Output Voltage, V_{OL}	C_{POL} = 0.1µF; I_{OL}= +1uA	0.05	0.4	V (max)
H / HV Polarity (Pin2) High Level Output Voltage, V_{OH}	C_{POL} = 0.1µF; I_{OL}= -1uA	4.5	4	V (min)
FVC Gain	22kHz ≤ f_H ≤ 110kHz	0.055		V/kHz
VCO Gain	22kHz ≤ f_{VCO} ≤ 110kHz	18.2		kHz/V
Phase Detector 1 Gain	H Sync Duty Cycle = 10%, f_H=110kHz	120		µA/radian
	f_H = 60kHz	80		
	f_H = 22kHz	30		
Phase Detector 1 Output Impedance (Pin12)		20		kΩ
Phase Detector 1 Leakage Current + VCO Bias Current (Pin12)	H / HV Sync Input Grounded	0.3	2	µA
Jitter	f_H = 110kHz (Note 8)	0.9		ns p-p
	f_H = 90kHz	1.1		
	f_H = 60kHz	1.6		
	f_H = 31kHz	3.6		
	f_H = 22kHz	5.8		
Free Run Frequency Variation	I_1 = -225µA	32	34	kHz (max)
		26	25	kHz (min)
H- Drive Phase Control, Gain	V_{10} = 2V to 6V (Note11)	8.89 (32)		% T_H/V (°/V)

Electrical Characteristics (Continued)

T_A = 25°C, V_{CC} = 12V, V_5 = 0V unless otherwise stated.

Parameter	Condition	Typical (Note 6)	Limit (Note 7)	Units
H Drive Phase Control Range	V_{10} = 3.6V to 7V (Notes 9 and 11)	± 14		% T_H
H Drive Duty Cycle Control Gain	V_4 = 0V to 4V (Note 10)	10.8		%/V
H Drive Duty Cycle Maximum (Pin 7)	V_4 = 0V (Note 10)	68	63	% (min)
H Drive Duty Cycle Minimum (Pin 7)	V_4 = 4V (Note 10)	25	35	% (max)
H Drive Low Level Output Voltage (Pin 7)	I_{OL} = 100mA	0.7		V
Flyback Input Threshold Voltage (Pin 6)	Positive-Going Flyback Pulse	2.2		V
Maximum Allowable Storage Delay of Horizontal Deflection Output Transistor Puls Half of Flyback Pulse Width	Fom H Drive Rising Edge to Center of Flyback Pulse	30		%T_H
V_{CC} Lockout Threshold Voltage (Pin 14)	V_{CC} Below Threshold: H Drive Output Disabled		8.5	V(max)
	V_{CC} Above Threshold: H Drive Output Enabled		10.5	V(min)
X-Ray Shutdown Threshold Voltage (Pin 5)	Above Threshold: H Drive Output Disabled	1.85	2	V(min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictaded by T_{JMAX} , Θ_{JA} and the ambient temperature, T_A . The maximum allowable power dissipation at any elevated temperature is $P_D = (T_{JMAX} - T_A) / \Theta_{JA}$ or the number given in the Absolute Maximum Ratings, which is lower. For this device, T_{JMAX} = 150°C. The typical thermal resistance (Θ_{JA}) of the LM1290N is 75°C/W.

Note 5: Human Body Model, 100pF capacitor discharged through a 1.5kΩ resistor.

Note 6: Typical specifications are the T_A = 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National AOQL (Average Outgoing Quality Level).

Note 8: The standard deviation, σ , of the flyback puls period is measured with a HP53310A Modulation Domain Analyzer. Peak-to-peak jitter of the flyback pulse is defined by 6σ.

Note 9: A positive phase value represents a phase lead of the flyback pulse peak with reference to the center of H sync.

Note 10: The duty cycle is measured under the conditions of free run with I_1 = -100µA, T_{FBP} = 3µs and T_D = 3.5µs where T_{FBP} and T_D are the flyback pulse width and the turn off delay of the H deflection output transistor respectively.

Note 11: T_H is defined as the total time of one horizontal line.