

Silicon Darlington Transistor

2SD560 / D560

100V/5A

DATASHEET

OEM – Fujitsu

Source: Fujitsu Databook 1983

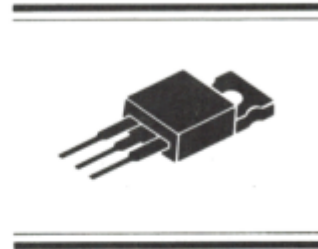
FUJITSU MICROELECTRONICS

2SD560

SILICON NPN EPITAXIAL DARLINGTON TRANSISTOR 5 AMP, 100 VOLT

DESCRIPTION

The 2SD560 is a low cost Darlington array which is perfectly suited for increasing TTL levels to drive print hammers, solenoids or motors.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Condition	Value	Unit
Storage Temperature Range	T _{stg}		-55 ~ +150	°C
Junction Temperature	T _j		+150	°C
Collector-Base Voltage	V _{CB0}		150	V
Emitter-Base Voltage	V _{EB0}		7	V
Collector-Emitter Voltage	V _{CEO}		100	V
Collector Current-Continuous	I _C		5	A
Collector Current-Peak	I _{CP}	P _W ≤ 10 ms, D.R. ≤ 50 %	8	A
Base Current	I _B		0.5	A
Collector Power Dissipation	P _C	T _a = 25 °C	1.5	W
	P _C	T _c = 25 °C	30	W

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

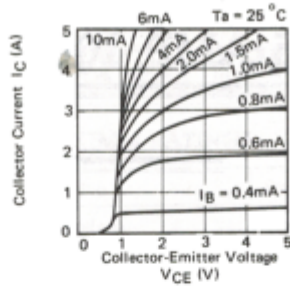
Characteristic	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I _{CB0}	V _{CB} = 100 V, I _E = 0	—	—	1	μA
DC Current Gain	h _{FE1}	V _{CE} = 2 V, I _C 3 A*	2000	4000	15000	—
	h _{FE2}	V _{CE} = 2 V, I _C = 5 A*	500	—	—	—
Collector-Emitter Saturation Voltage	V _{CE(sat)}	I _C = 3 A, I _B = 3 mA*	—	1.2	1.5	V
Base-Emitter Saturation Voltage	V _{BE(sat)}		—	1.6	2.0	V
Turn On Time	t _{on}	I _C = 3 A, I _{B1} = -I _{B2} = 3 mA R _L = 16.7 Ω, V _{CC} = 50 V Test Circuit	—	0.5	—	μs
Storage Time	t _{stg}		—	1.0	—	μs
Fall Time	t _f		—	1.0	—	μs

* Pulsed P_W ≤ 350 μs,
Duty Ratio ≤ 2 %

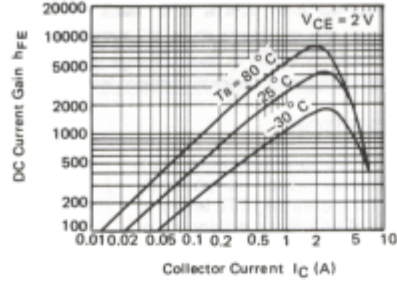
PACKAGE TYPE: TO-220. See page 5-23 for dimensions.

2SD560

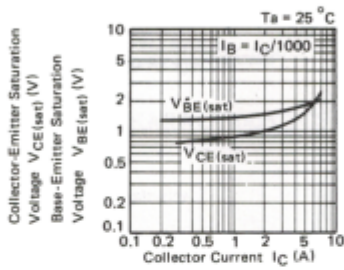
OUTPUT CHARACTERISTICS



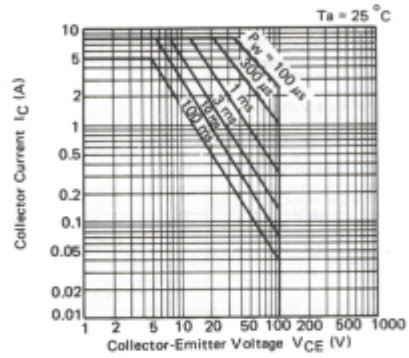
DC CURRENT GAIN



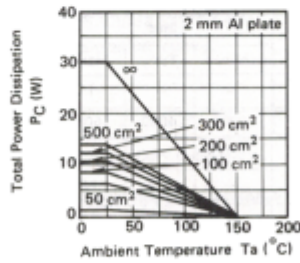
SATURATION VOLTAGE



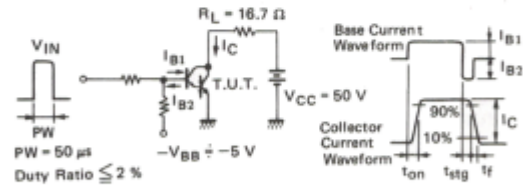
SAFE OPERATING AREA



TOTAL POWER DISSIPATION



SWITCHING TIME TEST CIRCUIT



TRANSISTOR PACKAGING INFORMATION

